A Novel Approach of Fiber Channel Switch for Avionics Applications.

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ABSTRACT*:   Developing the fiber channel switch specific to avionics application that supports various protocols. To achieve required size and power that are of custom made. Continued progress in both civil and military avionics applications is overstressing the capabilities of existing radio-frequency (RF) communication networks based on coaxial cables on board modern aircrafts. Future avionics systems will require high-bandwidth on-board communication links that are lightweight, immune to electromagnetic interference, and highly reliable. Fiber optic communication technology can meet all these challenges in a cost-effective manner. Recently, digital fiber-optic communication systems, where a fiber-optic network acts like a local area network (LAN) for digital data communications, have become a topic of extensive research and development. Although a fiber-optic system can be designed to transport radio-frequency (RF) signals, the digital fiber-optic systems under development today are not capable of transporting microwave and millimeter-wave RF signals used in radar and avionics systems on board an aircraft. Recent advances in fiber optic technology, especially wavelength division multiplexing (WDM), has opened a number of possibilities for designing on- board fiber optic networks, including all-optical networks for radar and avionics RF signal distribution. The relative merits and demerits of each architecture are discussed, and the suitability of each architecture for particular applications is pointed out. All-optical approaches show better performance than other traditional approaches in terms of signal-to-noise ratio, power consumption, and weight requirements.*

***KEYWORDS:*** *Fiber Channel Switch, RF(Radio Frequency), QE8 Registers , Lan*

I.   INTRODUCTION:

In Aircrafts, we have Radars and Sensors, used to collect the information regarding Climate, Obstacles etc. This information has to be processed and corresponding signals has to be given to pilot. The QE8 is a high-performance PCI Express quad-function 2, 4 or 8 gigabits per second Fibre Channel (FC) controller for host bus adapters and embedded subsystems. On the backplane of a host bus adapter, the QE8 interfaces directly to an industry standard PCI Express interface (PCI Express Gen I supports 2.5 gigabits per second, and Gen II supports 5.0 gigabits per second). On the front plane, each function can be independently configured to use the integrated 2, 4 or 8 gigabits per second Ser Des.

Recent advances in avionics applications in both civil and military aircrafts require high-bandwidth on-board microwave and millimeter-wave radio-frequency (RF) communication networks. A number of RF systems with their interconnection networkbased on coaxial cables and waveguides increase the complexity of the RF communication network on board modern civil and military aircrafts with increasing problems related to electromagnetic interference (EMI). A simple, reliable, and lightweight communication system that is free from the effects of EMI, and capable of supporting broadband RF communications needs of the future on-board avionics systems cannot implemented by existing coaxial cable based systems easily. Fiber-optic communication systems can meet all the challenges of modern avionics applications in an efficient and cost-effective manner where a single fiber has the potential to replace dozens of RF cables. In addition, a number of optical fibers can be bundled in a single fiber-optic cable, which has the potential to reduce the weight of the fiber significantly. In addition, fiber-optic components for airborne applications which are capable of withstanding the adverse environmental conditions on-board an aircraft are already under development [1].Presently, two different optical wavelength regions are used for modern optical communication in optical fiber. For both of these wavelengths two methods can be used for fiber-optic transmission: analog and digital. Analog signals are continuously varying signals where the exact waveform of the RF signal needs to be preserved when transmitted over a fiber optic link. This requires the analog fiber-optic transmitter and the analog fiber-optic receiver to be extremely stable, linear, and to have a large dynamic range.

These stringent requirements increase the cost of analog fiber optic transmitters and receivers considerably. On the other hand, digital signals are composed of ones and zeros as in computers. The digital signal does not require preserving the exact waveform of the transmitted signal as long as the transmitted signal is not distorted to the extent that ones and zeroes can not be distinguished from each other. For these reasons, digital fiber-optic communication equipment can perform well even when noise and distortion of the optical signal is present. Fiber-optic communication networks onboard aircrafts for digital data communication has recently become an active area of research and development.Analog fiber-optic links can be employed to transport microwave and millimeter-wave RF signals from one place to another on board an aircraft. These analog fiber-optic links take as input an RF signal, transports it over fiber, and reproduces at the output an exact replica of the RF waveform fed to it at the input end. The RF signal itself may be modulated by a baseband signal by any of the analog or digital modulation techniques, but an analog fiber-optic link transmits the RF signal in the same manner irrespective of the method of modulation used for modulating the RF signal by the baseband signal.
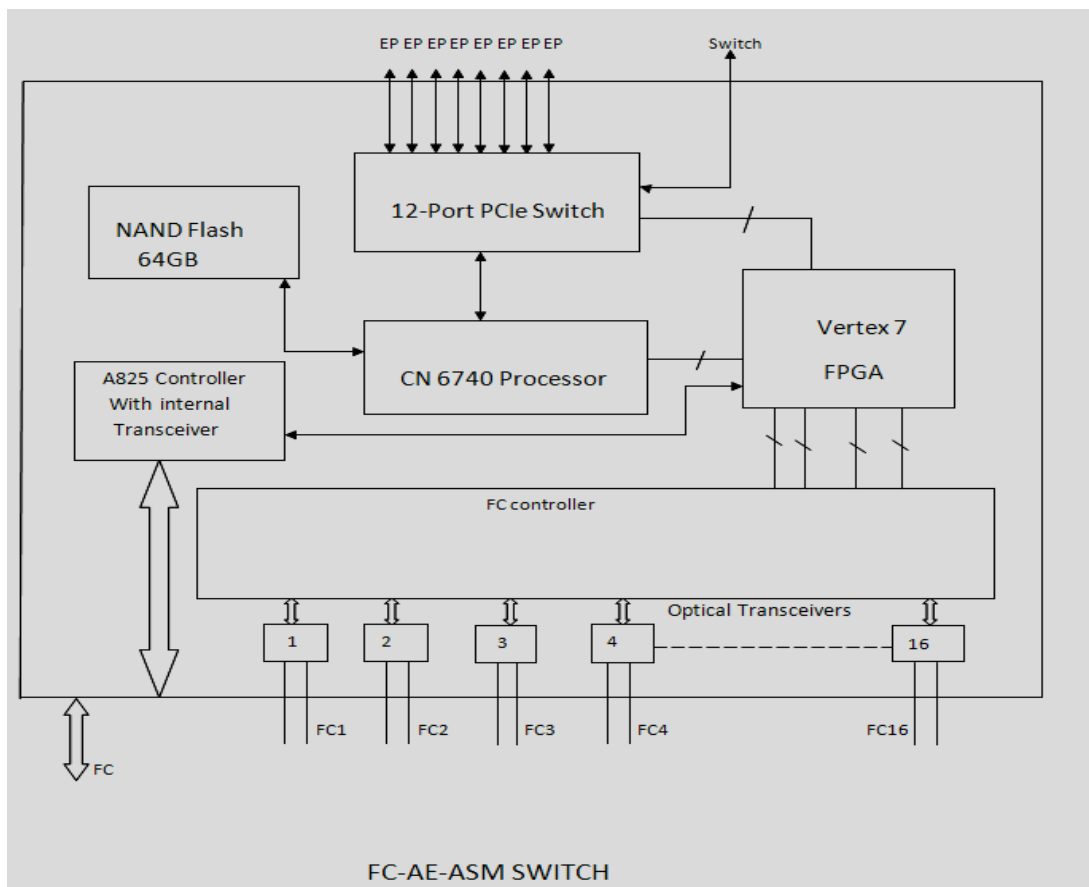
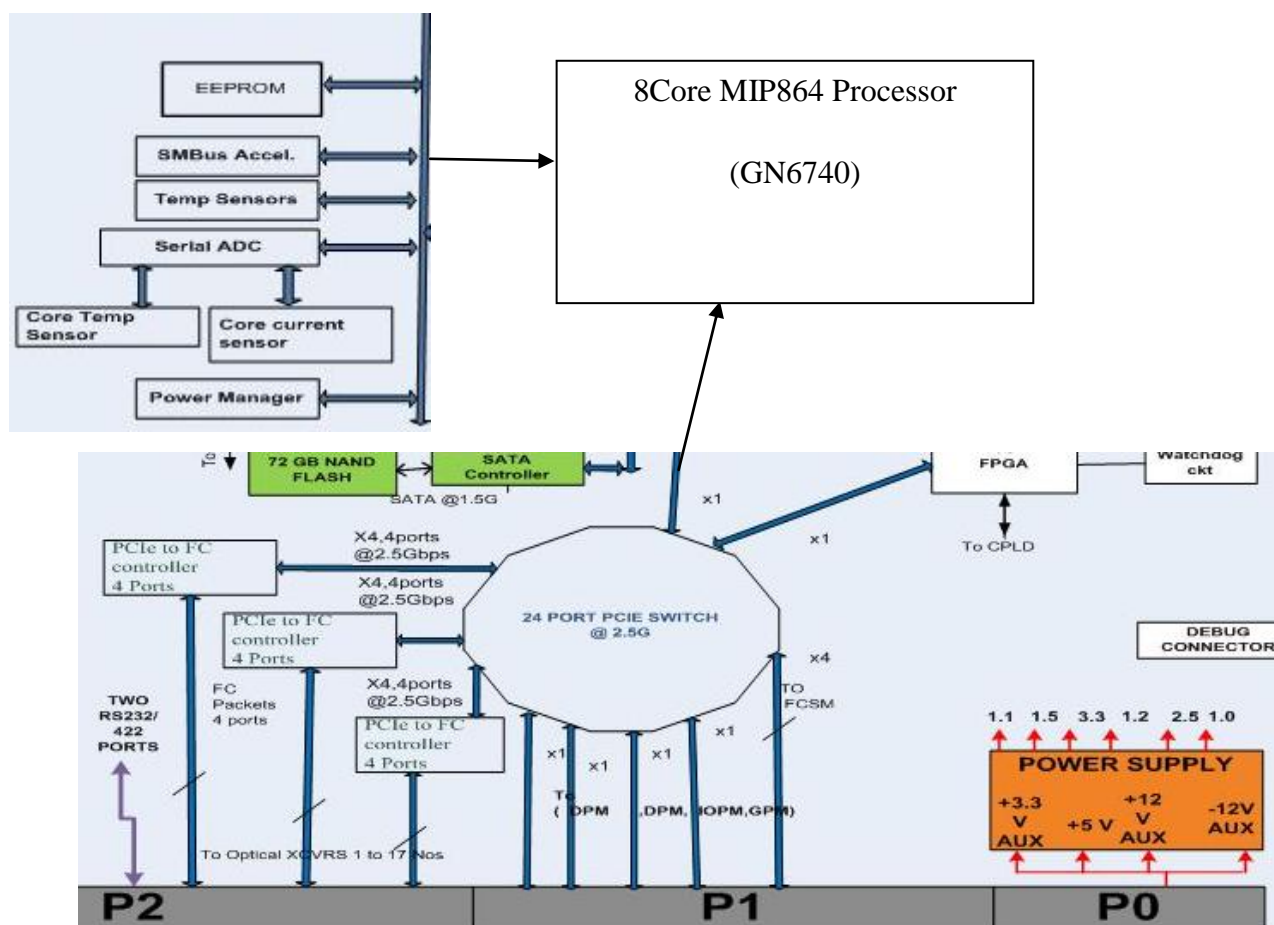**Figure 1: Block diagram of Switch**

Figure 2: Fiber Channel Switching Block Diagram.

Avionics architectures are evolving from "Federated" systems consisting of highly specialized black boxes connected together via MIL-STD-1553 PCI to FC Controller four ports and ARINC 429 data buses to "Integrated" and "Distributed" architectures. These new   architectures contain high data-rate sensors, parallel processors, and shared memory with high levels of integration. These systems require a new interconnection system that overcomes the limitations of older standards. Fibre Channel is a family of ANSI standards that define an interconnection system well suited to this task. This paper evaluates Fibre Channel as an avionics interconnection standard [2]. It begins by defining the requirements and measures of performance for an interconnection system suitable for the new avionics architectures. The requirements address technical performance, affordability, reliability, sustainability, and maintainability considerations. The Fibre Channel standards are then briefly compared to the   requirements for the avionics interconnection system. It is shown that a switched fabric Fibre Channel system can meet the requirements. evaluation of a switched fabric avionics interconnection systems.

II.   OVERVIEW OF QE8 REGISTERS
The QE8 supports four independent PCI Express functions. The QE8 device contains the follow-ing types of registers:PCI Express functional registers , Frame Manager registers and COE registers, Fibre Channel physical layer registers & PCI Express physical layer registers Functional registers include all registers that ar e not PCI Express registers or PCI Express Inter-face Manager registers. The structure of Memory Addressed registers are shown in fig3. There is a unique set of registers for each QE8 core function. Within each function, there is a unique set of registers for each Multiprocessor System (MPS). Since resources are shared across

MPSs, some registers are 'local' to the MPS and some are 'global'. The 'global' registers and bits are shared by the MPSs and are unique to a function. COE registers (COQ, CMQ, COE) are accessible only through Function 0. All registers are 32 bits., All registers must be accessed as full DWords.

NOTE: Attempts by the host to write individual bytes via byte enables will result in Target Aborts on PCI Express, and the setting of the UBE bit in the PCI Express Interrupt Status register. UBE, like other PCI Express non-parity errors, will cause the corresponding function to go fatal, and fatal error recovery will need to be initiated.

All registers have a power-on /reset value of 0 unless otherwise specified, All register accesses by the host are 32 bits in width., All registers may be mapped to PCI Express memory space, PC I Express I/O space, or both. MPSs 1 through 3 cannot be accessed through PCI Express I/O space; they are accessible through PCI Express memory space only

2.1 QE8 Programming Interface
The QE8 is a multi-function device and responds to functions 0 through 3 for configuration cycles. All PCI Express registers are byte accessible. However, the Fibre Core and COE registers may only be accessed as complete four-byte values.Writes to reserved registers ha ve unspecified consequences. Reads of reserved registers or address space will return undefined data. All PCI Express configuration space registers (excluding PCI Express Extended Configura-tion registers) are located in configuration as well as memory space. Each function maintains a complete set of PCI Express and Fibre Core registers. Function 0 specific registers are completely independent from Function 1, Function 2 and Function 3 specific registers (i.e. each function's registers can be independently programmed, but the definition for each register is exactly identical). COE register s are available only for Function 0. The QE8 requests a 32kB memory size, per function for registers. Multiprocessor Systems 1 through 3, MSI-X Table/PBA (Pending Bit Array) and COE registers are not accessible through IO space.
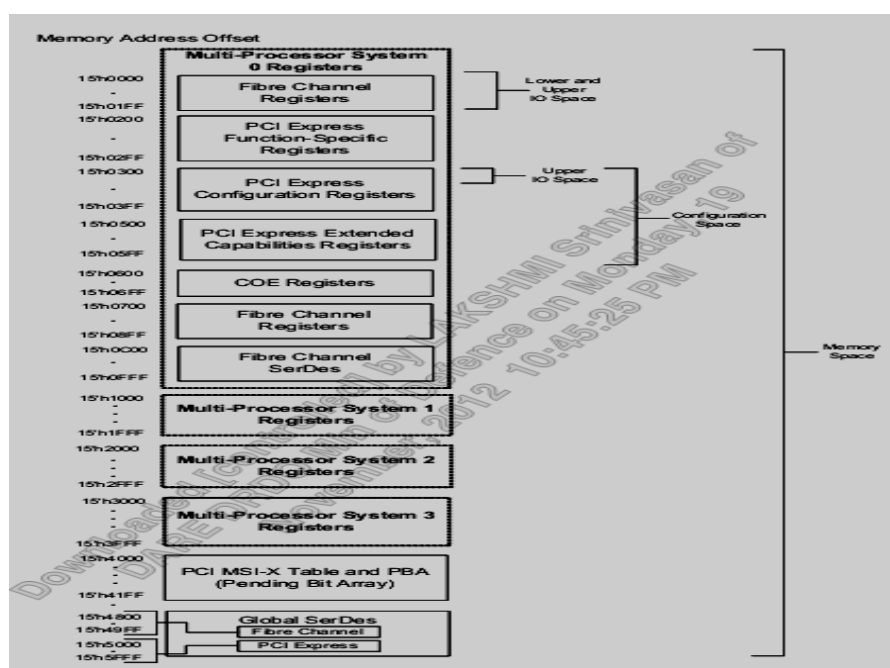

Figure 3: Register Resource mapping of QE8

Avionics systems can be characterized as real- time embedded systems. They contain multiple sensors generating data at high rates. This data is processed and displayed to the crew via multiple video displays and audible announcements. Often the timeliness and accuracy of this data is critical to the mission and to safety concems. These characteristics drive the technical requirements for an avionics interconnection system. The resulting technical requirements include: Bandwidth or throughput Number of communication nodes Latency,Determinism,Priority control Error detection, Confirmation of delivery, Time synchronization Reliability & Redundancy
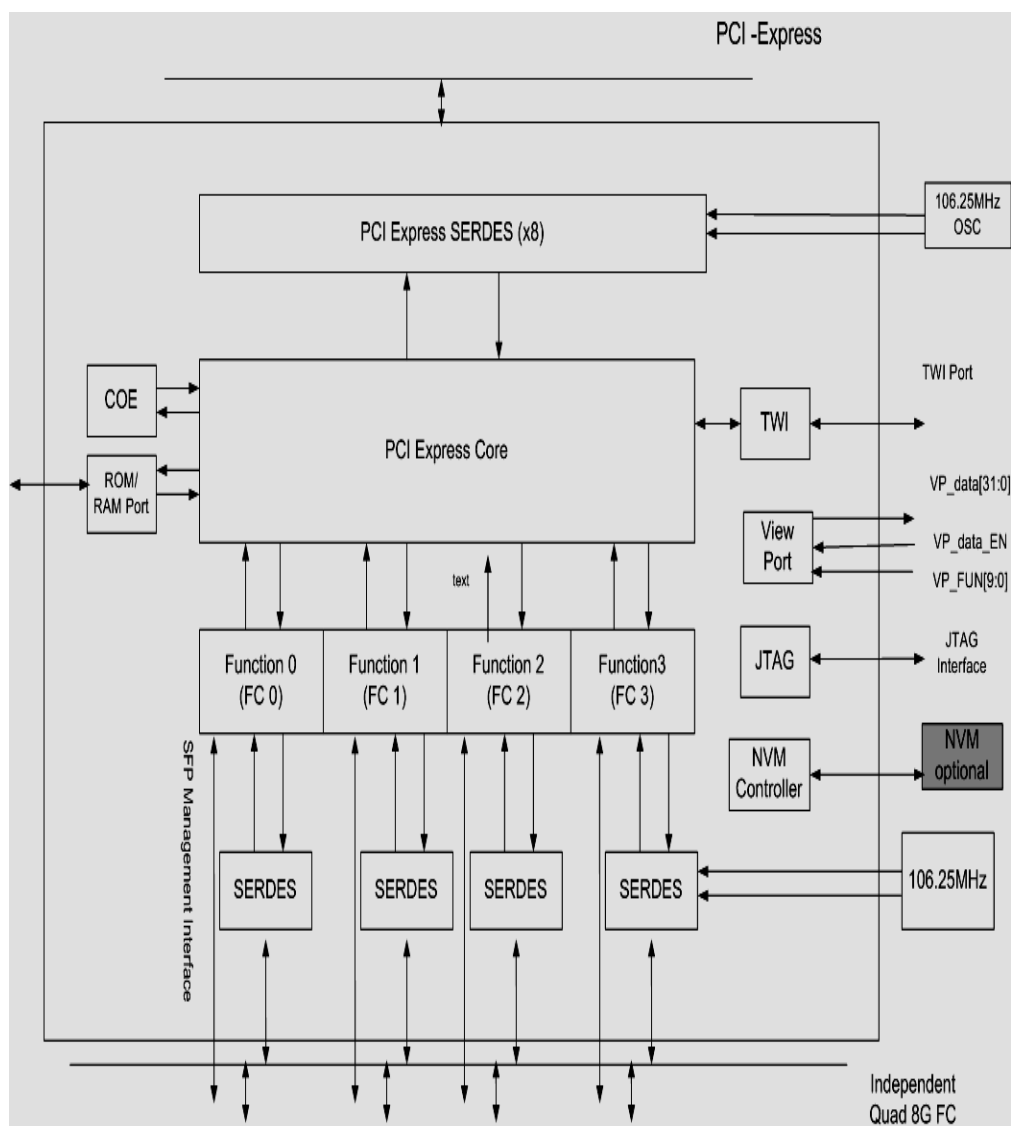
Internal Block Diagram.

Program the QE8 registers and PCIE express configuration registers. Build the data structures and inform the QE8 registers where they are located: IMQ ,SFQ, ERQ, SEST, HPQ Optional Initialization of Coe Initialization of Frame Manager.

2.3 Configuration of QE8 Pins

Table 1: Configuration of QE8 Pins a Shown Bellow:

Configuration	Status of Pin	Description
1. CFG(0)	active high---→ pull up Active low--	schmitt trigger input
2. CFG(1)	low----→ pull up	schmitt trigger inputs
3. CFG(2)	high---→ pull down	schmitt trigger inputs
4. CFG(3)	low--→ pull up	schmitt trigger inputs
5. .CFG(4):	high--→ pull down	Schmitt trigger inputs.
6. .CFG(5)	low---→ pull up	Schmitt trigger inputs.
7. CFG(6)	high--→ pull down	Schmitt trigger inputs
8. CFG(7)	low----→ pull up	Schmitt trigger inputs.
9. CFG(8)	high---→ pull down	Schmitt trigger inputs.
10. CFG(9)	low----→ reserved	
11. CFG(10):	low---→ reserved	
12. CFG(11)	low---→ reserved	
13. CFG(12):	low---→pull down	we can use all functions(fc0,fc1,fc2,fc3)
14. CFG(13)	low---→pull down	we can use all functions(fc0,fc1,fc2,fc3)
15. PCIE_RXPL	high---→ loads	default SerDes settings on deassertion of reset.
16. PCIE_EMPH:	high---→ loads	default SerDes settings on deassertion of reset.
17. CIE_RXEQ:	high---→ loads	default SerDes settings on deassertion of reset.
18. PCIE_LSA: reset.	high---→ loads	default SerDes settings on deassertion of
19. PCIE_VTX	high---→ loads	default SerDes settings on deassertion of reset.
20. PCIE_RXDIS:	no connection	Leave unconnected (default usage) when PCI Express compliant receiver terminations are connected to QE8 lane transmitters.
21. PCIE_GEN1_ONLY	high	supports link speed (2.5Gb/s to 5Gb/s)
22. PCIE_LOAD	High	loaded from the Parallel Memory Interface.
23. PCIE	low	separate reference clk

Basic Power Calculations For Fiber Channel
 The power dissipated by each and every component used in the module is calculated, which provides the heat dissipated by the entire module. According to the value, the heating sinking is provided to the module

Sl No	Part No	Quantity	Description	Package	Thermal resistance junction to case(θjC)	Thermal resistance junction to PCB(θjB)	Thermal resistance junction to ambient (θjA)	Power
1	MSM-096-B-M-2-L-M-00I	1	72 GB NAND FLASH	524 pin BGA	27°C/W	18.6°C/W		3.6W
2	HI-3113PCMF	1	Avionics CAN Controller with integrated Transceiver	44 PIN PLASTIC QFN (44PCS) PC (HI-3113 only)				0.085275W
3	89H32NT24AG2ZCHLGI	1	IC,32-Lane 24-Port PCIe System Interconnect Switch	484-Flip chip BGA				5.45w
4	W3J256M72G-1066PBI	1	2 GB DDR3 SDRAM	375 Plastic Ball Grid Array(PBGA)				10.34W
5	PM8032	3	Quad-Channel 8 Gbps Fibre Channel Protocol Controller (with Encryption)	480 Pin FCBGA-NH(Flip chip Ball Grid Array No Heatspreader)	0.056°°C/W	9.17C/W	19.69°C/W	6.06W
6	PM8001B-F3EI-P	1	8-Port 6 Gbit/s SAS/SATA Protocol Controller	Low-cost 672-pin 27 x 27 mm FCBGA package				6.19W
7	XC5VLX330T-3FFG1738I	1	Virtex5	FF1738(Flip-Chip Fine-pitch BGA)				15W
8	CN67401200BG1936-AAP	1	Processor	1936-pin FC-BGA	0.2°C/W	1.5°C/W		41.36W

Table 2: Thermal analysis

INPUT	REGISTER VALUE
000	C00000FF
001	00015C81
010	0C12
011	00000000
100	0041
101	300000E0
110	00000098

Table 3: Set of register input values

The Above Table shows the Corresponding Inputs and corresponding register values

III.   RESULTS:

A) The bellow simulation results are generated in Xilinx the register input value is **'001'** based on RTl stimulated results are shown bellow:
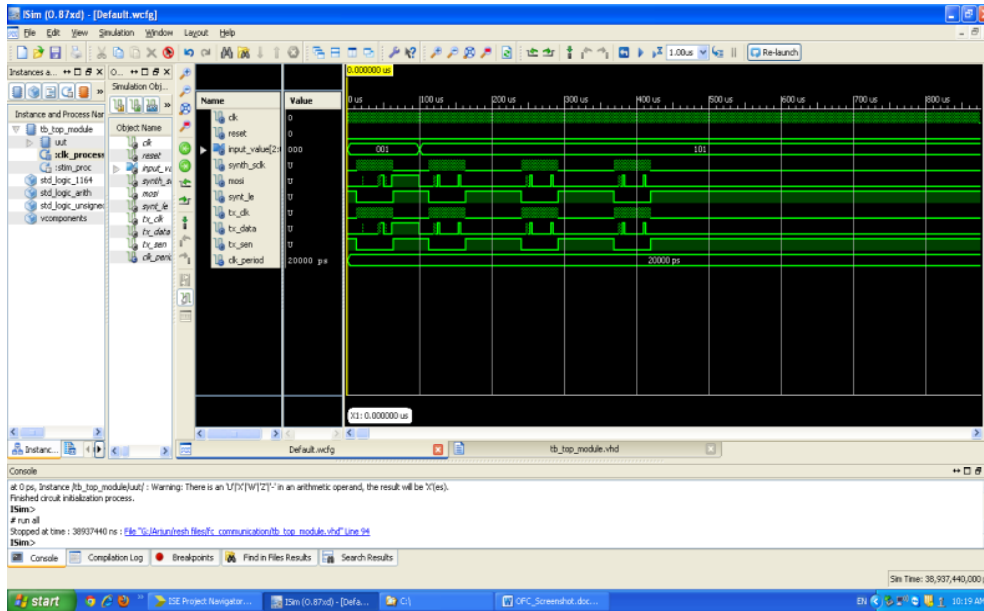

Fig5: corresponding output signal for the input 001

b) The bellow simulation results are generated in Xilinx the register input value is '**101**' based on RTl stimulated results are shown bellow:
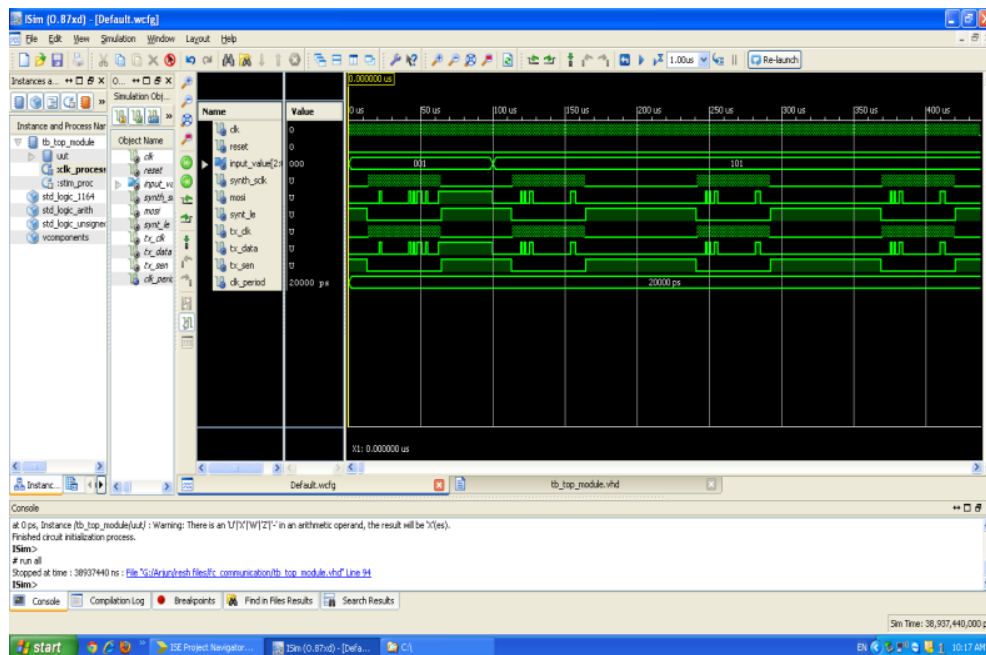

Fig6: corresponding output signal for the input 101

IV.   CONCLUSION:

Finally, the fiber channel switch specific to avionics application has been developed by achieving proper size and power that are custom was made a typical avionics system architecture ha s been designed as a federated architecture of black - boxes with   well - defined functions and implemented on fully dedicated Avionic Systems. The new Integrated Modular Avionic s (IMA) architecture relies on an architecture more similar to conventional computers, where several general -purpose processors are connected through a bus and all the Inputs/Outputs (I/O) com e from th e I/ O units (like Remote Interf ace Units , RIUs) through the bus to the processors. This architecture imposes a heavy traffic on data networks, as on the initial research Fibre Channel appears to be suitable for use in the advanced avionics architectures that will be found in future military aircraft. Bandwidth appears sufficient, guaranteed delivery is supported, and the device address space is sufficiently large.

REFERNCES:

[1]   RINC Specification 653. Avionics Application Software Standard Interface. 2005
[2]   B.L. Di Vito, "A formal Model of Partitioning for Integrated Modular Avionics", NASA/CR-1998-208703,
[3]   August 2006.
[4]   G. Romanski, "High Integrity Software for High Integrity Systems", SIGAda 2000.
[5]   Tom Bohman, Systran Corporation, "Fibre Channel Network Technology Applied to Advanced DSP Systems", 2007.
[6]   Kembel, Robert W., 2008, Comprehensive Introduction to Fibre Channel, Tucson, AZ, Northwest Learning Associates.
[7]   Pinney, Lt Col Chuck, 2004, Joint Advanced Strike Technology Program, Avionics Architecture
[8]   Definition, Version 1.0, Arlington, VA.